WHAT IS CLAIMED IS:

1. A receive path circuit in a radio frequency (RF) receiver comprising:

a local oscillator (LO) circuit capable of receiving a local oscillator (LO) reference signal having frequency, LO, and a double sideband (DSB) clock signal having a frequency, DSB, and generating therefrom an in-phase product signal of said LO reference signal and said DSB clock signal in which a polarity of said LO reference signal is reversed at said DSB frequency of said DSB clock signal; and

a first radio frequency (RF) mixer having a first input port capable of receiving said in-phase product signal from said LO circuit and a second input port capable of receiving a modulated radio frequency (RF) signal, wherein said first RF mixer generates a first downconverted output signal.

2. The receive path circuit as set forth in Claim 1 wherein said LO circuit is further capable of generating a quadrature phase product signal from said LO reference signal and said DSB clock signal, wherein said quadrature phase signal is shifted approximately 90 degrees with respect to said in-phase product signal and wherein a polarity of said LO reference signal is reversed at said DSB frequency of said DSB clock signal.

3. The receive path circuit as set forth in Claim 2 further comprising a second radio frequency (RF) mixer having a first input port capable of receiving said quadrature phase product signal from said LO circuit and a second input port capable of receiving said modulated radio frequency (RF) signal, wherein said second RF mixer generates a second downconverted output signal.

4. The receive path circuit as set forth in Claim 3 wherein said LO circuit comprises a multiplier that receives an in-phase LO reference signal and said DSB clock signal and generates therefrom said in-phase product signal.

5. The receive path circuit as set forth in Claim 4 wherein said multiplier is an analog multiplier.

6. The receive path circuit as set forth in Claim 4 wherein said multiplier is an exclusive-OR gate.

7. The receive path circuit as set forth in Claim 3 wherein said first downconverted output signal of said first RF mixer is a double-sideband suppressed carrier signal.

8. The receive path circuit as set forth in Claim 7 wherein said second downconverted output signal of said second RF mixer is a double-sideband suppressed carrier signal.

9. The receive path circuit as set forth in Claim 8 further comprising a first DSB filter block capable of receiving said first downconverted output signal from said first RF mixer and said DSB clock signal, wherein said first DSB filter block reverses a polarity of said first downconverted output signal at said DSB frequency of said DSB clock signal to thereby produce an in-phase baseband output signal.

10. The receive path circuit as set forth in Claim 9 further comprising a second DSB filter block capable of receiving said second downconverted output signal from said second RF mixer and said DSB clock signal, wherein said second DSB filter block reverses a polarity of said second downconverted output signal at said DSB frequency of said DSB clock signal to thereby produce a quadrature phase baseband output signal.

11. A radio frequency (RF) receiver comprising:

a receiver front-end circuit capable of receiving an incoming RF signal from an antenna and filtering and amplifying said incoming RF signal;

a local oscillator (LO) circuit capable of receiving a local oscillator (LO) reference signal having frequency, LO, and a double sideband (DSB) clock signal having a frequency, DSB, and generating therefrom an in-phase product signal of said LO reference signal and said DSB clock signal in which a polarity of said LO reference signal is reversed at said DSB frequency of said DSB clock signal; and

a first radio frequency (RF) mixer having a first input port capable of receiving said in-phase product signal from said LO circuit and a second input port capable of receiving said filtered and amplified incoming RF signal, wherein said first RF mixer generates a first downconverted output signal.

12. The radio frequency (RF) receiver as set forth in Claim 11 wherein said LO circuit is further capable of generating a quadrature phase product signal from said LO reference signal and said DSB clock signal, wherein said quadrature phase signal is shifted approximately 90 degrees with respect to said in-phase product signal and wherein a polarity of said LO reference signal is reversed at said DSB frequency of said DSB clock signal.

13. The radio frequency (RF) receiver as set forth in Claim 12 further comprising a second radio frequency (RF) mixer having a first input port capable of receiving said quadrature phase product signal from said LO circuit and a second input port capable of receiving said filtered and amplified incoming RF signal, wherein said second RF mixer generates a second downconverted output signal.

14. The radio frequency (RF) receiver as set forth in Claim 13 wherein said LO circuit comprises a multiplier that receives an in-phase LO reference signal and said DSB clock signal and generates therefrom said in-phase product signal.

15. The radio frequency (RF) receiver as set forth in Claim 14 wherein said multiplier is an analog multiplier.

16. The radio frequency (RF) receiver as set forth in Claim 14 wherein said multiplier is an exclusive-OR gate.

17. The radio frequency (RF) receiver as set forth in Claim 13 wherein said first downconverted output signal of said first RF mixer is a double-sideband suppressed carrier signal.

18. The radio frequency (RF) receiver as set forth in Claim 17 wherein said second downconverted output signal of said second RF mixer is a double-sideband suppressed carrier signal.

19. The radio frequency (RF) receiver as set forth in Claim 18 further comprising a first DSB filter block capable of receiving said first downconverted output signal from said first RF mixer and said DSB clock signal, wherein said first DSB filter block reverses a polarity of said first downconverted output signal at said DSB frequency of said DSB clock signal to thereby produce an in-phase baseband output signal.

20. The radio frequency (RF) receiver as set forth in Claim 19 further comprising a second DSB filter block capable of receiving said second downconverted output signal from said second RF mixer and said DSB clock signal, wherein said second DSB filter block reverses a polarity of said second downconverted output signal at said DSB frequency of said DSB clock signal to thereby produce a quadrature phase baseband output signal.